As previously discussed, Jung specifically discloses that the extended portion 240 of the semiconductor layer is non-doped. A storage electrode 420 is connected to a storage line 430, and a pixel electrode 800 is electrically connected to the non-doped semiconductor layer 240 via contact electrode 620, doped semiconductor layer 230, and contact holes C2 and C3. A capacitor is thus formed between the non-doped portion 240 and storage electrode 420 via the gate insulating film 300. Another capacitor is also formed between storage electrode 420 and pixel electrode 800 via insulators 500 and 700.

According to the method taught by Jung, the storage electrode 420 is formed at the same time as the gate electrode 410. The doping process to the source/drain electrodes 210/230 is therefore performed by utilizing the gate electrode 410 and the storage electrode 420 as masks. According to this teaching therefore, semiconductor layer 240 under the storage electrode 420 can only be non-doped. In other words, the semiconductor layer 240 will not include impurity.

In contrast, claim 10 of the present invention features first and second semiconductor layers having impurity formed on both sides of the operating semiconductor layer. The first semiconductor layer with impurity thus acts as a first storage capacitor electrode. A second storage capacitor electrode is formed between the first and second insulating films, which are different from the gate insulating film, and connected to a storage capacitor wiring maintained at a predetermined potential. A first storage capacitor is therefore structured by the first storage capacitor electrode which has impurity, the first

insulating film which is different from the gate insulating film, and the second storage capacitor electrode. The second storage capacitor is therefore structured by the second storage capacitor electrode, the second insulating film, and the pixel electrode. Jung does not teach or suggest such a structure having all of these features.

Contrary to the Examiner's assertion, Jung does not teach both doped and undoped embodiments. As discussed above, all embodiments disclosed by Jung specifically teach a doped storage region 240. The Examiner even acknowledges on page 4 of Paper No. 8 that Jung only teaches that "the storage region 240 is not required to be doped." Such a negative inference alone, however, can by no means be considered an *explicit* disclosure of a doped embodiment, particularly given the fact that Jung never teaches any doped embodiments. Accordingly, a rejection under Section 102 based on Jung is wholly inappropriate in the present case, and should be withdrawn.

Similarly, claim 10 of the present invention would not be obvious from Jung when all of the disclosed embodiments teach away from having impurity in the semiconductor layers. In fact, the very portion of Jung cited by the Examiner (col. 8, lines 25-30) even further teaches away from the present invention. In this cited text section, Jung not only fails to teach a doped semiconductor layer, but also suggests away from having a doped semiconductor layer. The assertion that Jung must teach a doped embodiment, based solely upon the single teaching that the storage region 240 "is not required to be doped," is an unreasonable interpretation, which is not supported by the prior art reference. Accordingly,

for at least these additional reasons, the rejection of claim 10 of the present invention is further traversed.

Claim 11 stands rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (6,088,071). Claim 11 has been rewritten in independent form, and Applicant respectfully traverses.

Similar to the discussion above, claim 11 of the present invention has also been improperly rejected under Section 102. Yamamoto reveals doped and undoped embodiments, but does not disclose the same structure for both embodiments. In this regard, neither embodiment shows all of the features of the present invention.

Applicant submits that Yamamoto fails to disclose a first semiconductor layer having impurity used as a first storage capacitor electrode, a second storage capacitor electrode formed between first and second insulating films (different from the gate insulating film) and connected to a storage capacitor wiring maintained at a predetermined potential, where at least the first storage capacitor is structured by the first storage capacitor electrode (which has impurity), the first insulating film, and the second storage capacitor electrode. These features, together with a second storage capacitor structured by the second storage capacitor electrode, the second insulating film, and the pixel electrode, are neither taught nor suggested by Yamamoto. Because Yamamoto fails to disclose all of the features of the present invention within any single embodiment, the rejection under Section 102 is inappropriate, and should be withdrawn.

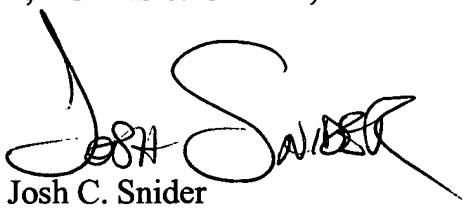
Claims 12-13 and 15 stand rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. (U.S. 5,182,661). Claim 12 has been rewritten in independent form, and has been further amended to include the allowable subject matter from claim 14, as indicated by the Examiner. Accordingly, claim 12 should be in condition for allowance, which is respectfully requested. Claims 13 and 15 depend from claim 12, and should also therefore be in condition for allowance by this amendment.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, captioned **"Version with Markings to Show Changes Made."**

For all of the foregoing reasons, Applicant submits that this Application, including claims 10-13 and 15, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

IN THE CLAIMS:

Claims 10-13 and 15 have been amended as follows:

10. (Thrice Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers having impurity formed on both sides of the operating semiconductor layer ~~including impurity~~, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer~~, and a drain electrode including the second semiconductor layer and connected to the data wirings~~ and the gate electrode; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

11. (Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers formed on both sides of the operating semiconductor layer, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window

opened to first and second insulating layers laminated on the first semiconductor and the gate electrode;

~~An active matrix type display as set forth in claim 10, wherein the first storage capacitor electrode uses~~ a an impurity semiconductor layer formed isolated from the first semiconductor layer on the substrate and made of the same material as the first semiconductor layer.; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

12. (Amended) An active matrix type display comprising:~~as set forth in claim 10, wherein a plurality of the storage capacitor electrodes have a third storage capacitor electrode formed on the first insulating film in the gate wiring area at a previous stage of the pixel area and connected to the pixel electrode in the pixel area, and a fourth storage capacitor electrode formed on the second insulating film in the gate wiring area and the data wiring area and providing an end of the pixel electrode formed on a third insulating~~

~~film formed at an upper portion and an end overlapping viewing the substrate perpendicularly, wherein a third storage capacitor is structured by the third storage capacitor electrode, the second insulating film and the fourth storage capacitor electrode, and the fourth storage capacitor is structured by the fourth storage capacity electrode, the third insulating film and the pixel electrode.~~

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a first, a second and a third insulating film formed on the gate wirings;

a pixel electrode formed in a pixel decided by the gate wirings and the data wirings:

a thin film transistor formed in the pixel and having a gate electrode connected to one of the gat wirings, a source electrode connected to the pixel electrode, and a drain electrode connected to the data wirings;

a first storage capacitor electrode formed between the first insulating film and the second insulating film in an area of the gate wiring for previous pixel to the pixel and connected to the pixel electrode; and

a second storage capacitor electrode also serving as a storage capacitor wiring formed between the second insulating film and the third insulating film in the area of the gate wiring;

wherein a first storage capacitor is structured by the first storage capacitor electrode, the second insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the third insulating film and the pixel electrode.

13. (Amended) An active matrix type display as set forth in claim 12, wherein a ~~fifth~~third storage capacitor is structured by the ~~third~~first storage capacitor electrode, the first insulating film and the gate wiring.

15. (Amended) An active matrix type display as set forth in claim 12, wherein the ~~fourth~~second storage capacitor electrode also serves as a shading film.